EE 203   Name _____
Exam 3
Spring 2006

Instructions: There are 10 questions on this exam that are worth 2 pts each and 5
problems worth 16 points each. Answer all questions and solve all problems. All work
should be included on the exam itself. Attach additional sheets only if you run out of
space on a problem. Students may bring 6 pages of notes to the exam. Calculators are
permitted but can not be shared.
        Unless stated to the contrary, assume all diodes are ideal, all MOS transistors are
from a process with $\mu_n C_{OX}$=100µA/V^2, $\mu_p C_{OX}$=33µA/V^2, V_{Tn}=1V, and V_{Tp}= -1V, and all
BJT transistors are from a process with J_S= 10^{-13}A/µ^2 , β=100 and V_{AF} = ∞ for both npn
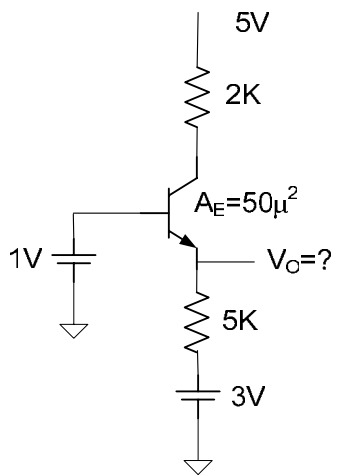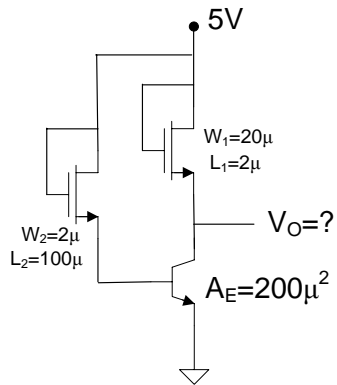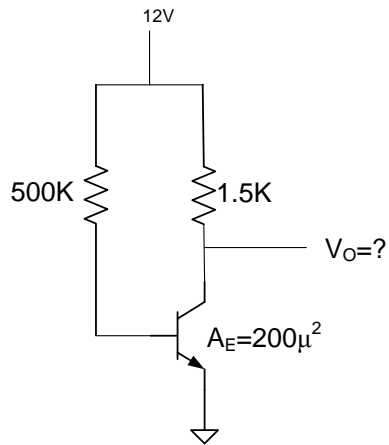and pnp transistors.

Questions:

1. In what year was the BJT first introduced?

2. What region of operation of the MOSFET corresponds to the Forward Active region
    of the BJT?

3. What is the major reason CMOS logic replaced NMOS logic?

4   The fan-in capacitance of a minimum-sized equal rise/fall CMOS inverter in a
process where μ_n/μ_p=3 and V_{TN}=-V_{TP} is C_{IN}=4$C_{OX}W_{min}L_{min}$ where W_{min} and L_{min} are the
minimum allowable width and length of transistors in the process. What is the fan-in
capacitance of a minimum-sized inverter in the same process?

5   The propagation delay (t_{HL}+t_{LH}) of an inverter driving an identical device in a
state of the art CMOS process is a few picoseconds yet the clock period on current
microprocessors is around a factor of 100 larger. What are the TWO major reasons the
clock speed on these processors is so much longer than the inverter pair propagation
delay?

6.   What are the two major benefits that Dynamic Logic gates offer?

7.   List the process parameters of a Bipolar Transistor?

8.   The bipolar transistor has some advantages when compared to the BJT and some disadvantages. What are the two major advantages of the BJT?

9.   What technology (CMOS or Bipolar) is used to fabricate the 741 Op Amp?

10. If a 1pF capacitive load is driven by a CMOS inverter operating with a single 2.5V power supply at a clock rate of 500MHz, what power will be dissipated in the inverter?

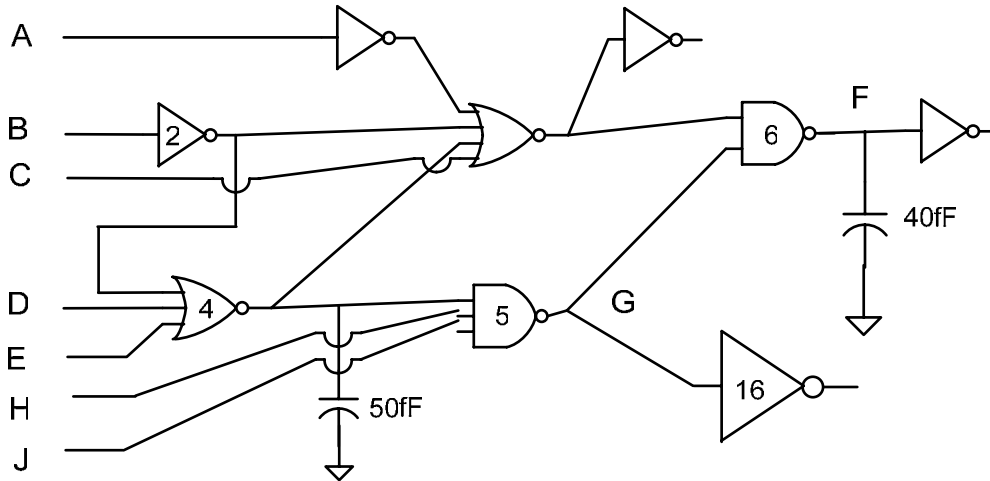Problem 1   Determine the variables indicated with a ?

12V

500K   1.5K

Vo=?

$A_E=200\mu^2$

5V

$W_1=20\mu$
$L_1=2\mu$

Vo=?

$W_2=2\mu$
$L_2=100\mu$

$A_E=200\mu^2$

5V

2K

$A_E=50\mu^2$

1V

Vo=?

5K

3V

Problem 2

The I_D-V_{DS} characteristics for an n-channel MOSFET are shown. Determine μC_{OX}, V_T and λ for this device. The width of the transistor was 10μ and the length was 2μ.
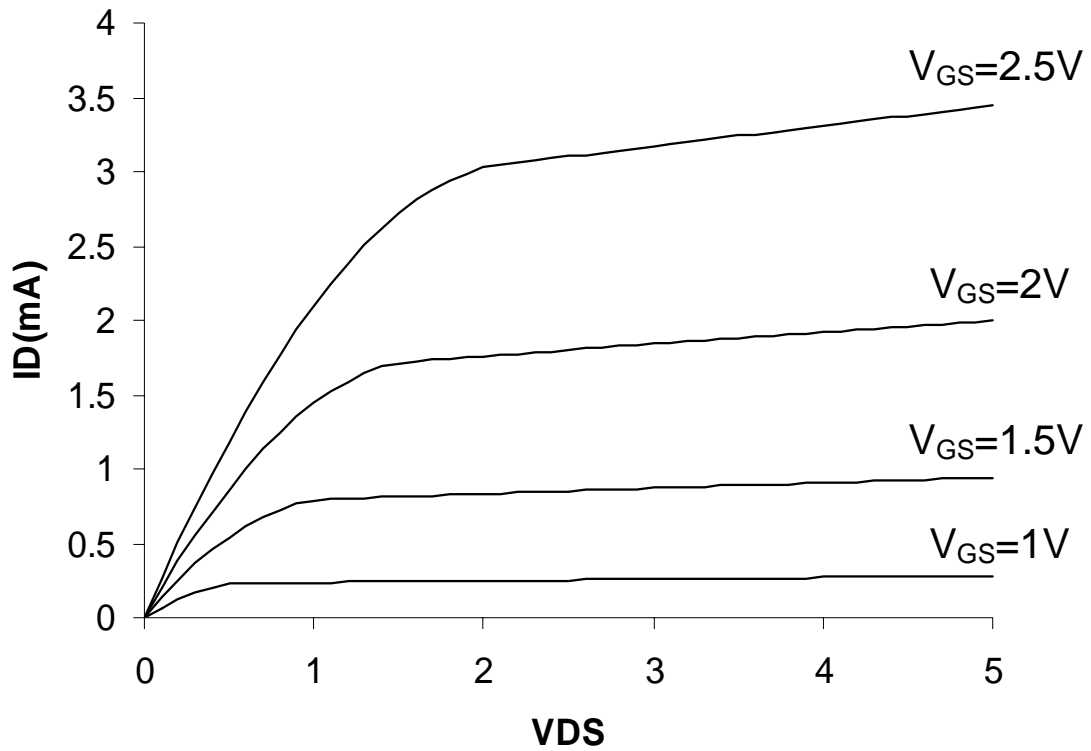
Problem 3   Determine the propagation delay from B to G. Assume all devices are sized for equal worst-case rise and fall time and that the overdrive of the gates, if different than 1, are as indicated. Assume you are working in a process wit V_{DD}=5V, V_{TN}=1V, V_{TP}=-1V, u_nC_{OX}=100uA/V^2, C_{OX}=4fF/u^2, Lmin = 0.25μ,Wmin = 0.25μ and μ_n/μ_p=3..

Problem 4

Design Boolean circuits at the transistor level that will implement the function

$F = A\overline{B} + BC + \overline{A}B\overline{C}$ with

  a)   Static CMOS
  b)   Complex Logic Gates
  c)   Pass Transistor Logic
  d)   Dynamic Logic

Assume the input variables A,B and C are available and that if compliments of variables are needed, generate them with Static CMOS inverters. You need not size the transistors.

Problem 5

For the circuit shown
- a) Determine the Boolean output function F
- b) Size the devices so that the worst-case pull-down resistance is 400Ω and the worst-case pull-up resistance is 800Ω.
- c) If sized as in part b), what will be the fastest and slowest LH output transition if C_L=500fF?
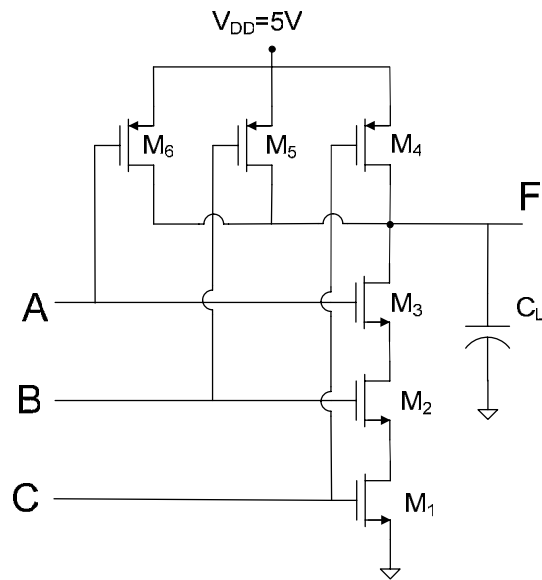
Exam 3
Spring 2006

Instructions: There are 10 questions on this exam that are worth 2 pts each and 5
problems worth 16 points each. Answer all questions and solve all problems. All work
should be included on the exam itself. Attach additional sheets only if you run out of
space on a problem. Students may bring 6 pages of notes to the exam. Calculators are
permitted but can not be shared.

       Unless stated to the contrary, assume all diodes are ideal, all MOS transistors are
from a process with $\mu_n C_{OX}=100\mu A/V^2$, $\mu_p C_{OX}=33\mu A/V^2$, $V_{Tn}=1V$, and $V_{Tp}= -1V$, and all
BJT transistors are from a process with $J_S= 10^{-13} A/\mu^2$, $\beta=100$ and $V_{AF} = \infty$ for both npn
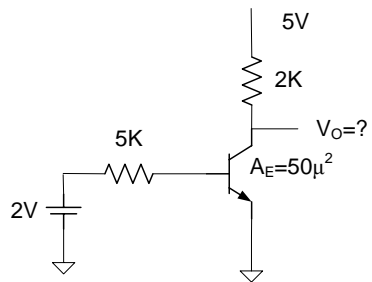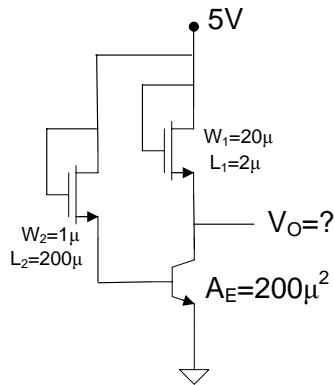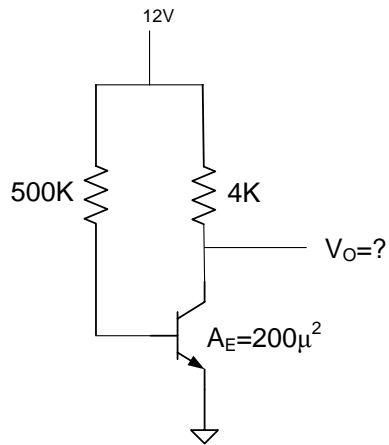and pnp transistors.

Questions:

1. In what year was the BJT first introduced?

2. What region of operation of the MOSFET corresponds to the Forward Active region
    of the BJT?

3. What is the major reason CMOS logic replaced NMOS logic?

4   The fan-in capacitance of a minimum-sized equal rise/fall CMOS inverter in a
process where $\mu_n/\mu_p=3$ and $V_{TN}=-V_{TP}$ is $C_{IN}=4C_{OX}W_{min}L_{min}$ where W_{min} and L_{min} are the
minimum allowable width and length of transistors in the process. What is the fan-in
capacitance of a minimum-sized inverter in the same process?

5   The propagation delay ($t_{HL}+t_{LH}$) of an inverter driving an identical device in a
state of the art CMOS process is a few picoseconds yet the clock period on current
microprocessors is around a factor of 100 larger. What are the TWO major reasons the
clock speed on these processors is so much longer than the inverter pair propagation
delay?

6.   What are the two major benefits that Dynamic Logic gates offer?

7.   List the process parameters of a Bipolar Transistor?

8.   The bipolar transistor has some advantages when compared to the BJT and some disadvantages. What are the two major advantages of the BJT?

9.   What technology (CMOS or Bipolar) is used to fabricate the 741 Op Amp?

10. If a 1pF capacitive load is driven by a CMOS inverter operating with a single 4V power supply at a clock rate of 200MHz, what power will be dissipated in the inverter?

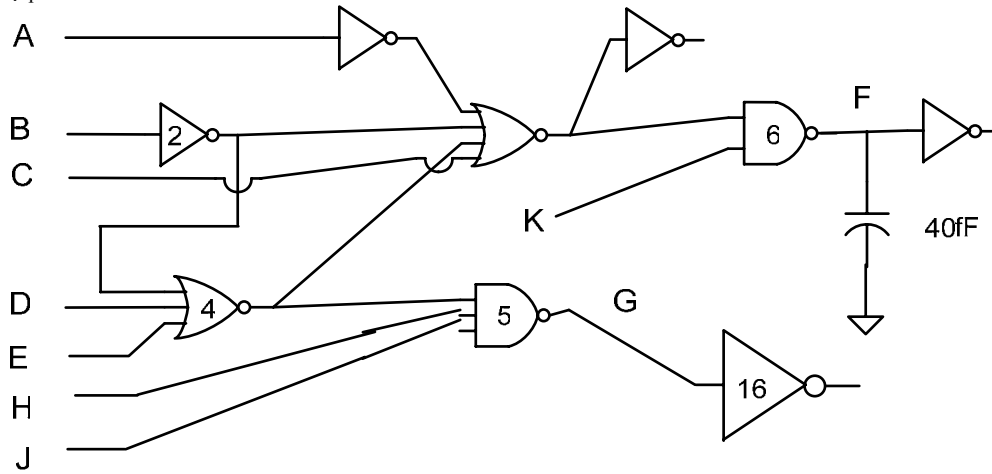Problem 1   Determine the variables indicated with a ?

12V

500K   4K

$V_O=?$

$A_E=200\mu^2$

5V

$W_1=20\mu$
$L_1=2\mu$

$V_O=?$

$W_2=1\mu$
$L_2=200\mu$

$A_E=200\mu^2$

5V

2K

5K $V_O=?$

$A_E=50\mu^2$

2V

Problem 2

The I_D-V_{DS} characteristics for an n-channel MOSFET are shown. Determine μC_{OX}, V_T and λ for this device. The width of the transistor was 5μ and the length was 2.5μ.
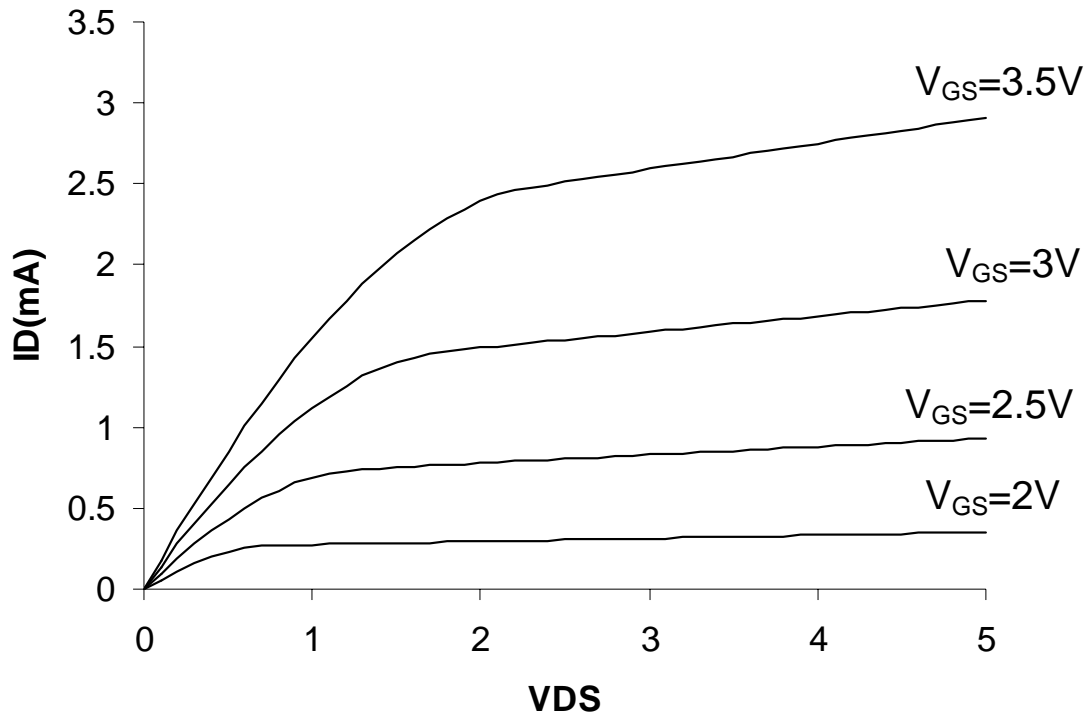
Problem 3   Determine the propagation delay from D to F. Assume all devices are sized for equal worst-case rise and fall time and that the overdrive of the gates, if different than 1, are as indicated. Assume you are working in a process wit V_{DD}=5V, V_{TN}=1V, V_{TP}=-1V, u_nC_{OX}=100uA/V^2, C_{OX}=4fF/u^2, Lmin = 0.25μ, Wmin = 0.25μ and μ_n/μ_p=3..

Problem 4

Design Boolean circuits at the transistor level that will implement the function

$F = A\overline{B} + B\overline{C} + \overline{A}\overline{B}C$ with

    a)   Static CMOS
    b)   Complex Logic Gates
    c)   Pass Transistor Logic
    d)   Dynamic Logic

Assume the input variables A,B and C are available and that if compliments of variables are needed, generate them with Static CMOS inverters. You need not size the transistors.

Problem 5

For the circuit shown
a) Determine the Boolean output function F
b) Size the devices so that the worst-case pull-down resistance is 400Ω and the worst-case pull-up resistance is 200Ω.
c) If sized as in part b), what will be the fastest and slowest LH output transition if C_L=200fF?